## REMARKS/ARGUMENTS

Claims 1-17 are pending in the application. Claims 1-17 are rejected. Claims 1, 6, and 9 have been amended.

Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §102 (e) as being anticipated by Shen et al. U.S. Patent No. 6,526,481 (Hereinafter "Shen"). Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp. 140-240 (Hereinafter "Handy"). Claims 16-17 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Handy and in further view of Witt et al. U.S. Patent No. 6,202,139 (Hereinafter "Witt").

### Claim Rejections under 35 U.S.C. § 102

Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §102 (e) as being anticipated by Shen. Shen discloses a methodology for designing a distributed shared-memory system. The distributed shared-memory system can incorporate adaptation or selection of cache protocols during operation. It guarantees semantically correct processing of memory instructions by the multiple processors. (*See* Abstract).

Applicants respectfully submit that Shen fails to disclose an integrated cache coherent device. Shen makes no mention of whether the memory system 120 is integrated into a single device or made of several different devices. In describing the architecture of the memory system 120, Shen implies many different devices are used. Shen states:

> Furthermore, the protocols are described in terms of FIFO communication channels between the instruction processors and the caches and between the caches and the shared

memory. These FIFO channels can be implemented by parallel or serial communication busses within an integrated circuit contained on a computer backplane or a message-passing network. The protocols described above can also be applied to distributed shared-memory systems in which caches and shared memory are on different computers coupled by a data network. This data network could be local, or could be a wide area network, such as the Internet. Note that implementation of the memory system, in general, includes implementation of multiple distributed components (individual caches and the shared memory) of the memory system which together provide a correct implementation in their combined behavior.

(Shen, col. 25, line 60 – col.26, line 9).

In other words, the memory system described in Shen encompasses either an entire computer or an entire network, and not an integrated device. Therefore claims 1, 6, and 9, are not anticipated by Shen. Accordingly reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. §102(b) is respectfully requested. In addition, Applicants respectfully submit that claims 2-4, 7-8, 10-12 and 14 are allowable as depending from allowable base claims 1, 6 and 9.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 1-4, 6-12, and 14 under 35 U.S.C. §102(b) is respectfully requested.

**Claim Rejections under 35 U.S.C. § 103**

Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Handy. Handy discloses a protocol for use in multiple processor system with multiple caches.

As discussed above, Shen does not disclose an integrated coherent cache device as recited in claims 1 and 9 as amended, and by their dependency claims 5, 13, and 15. Handy also does not disclose an integrated cache coherent device. Therefore Applicants respectfully submit that

claims 5, 13, and 15 are allowable as depending from allowable base claims 1 and 9 given the arguments above.

Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Handy and in further view of Witt. Witt discloses a pipelined data cache with multiple ports. The invention is described as a computer system including a processor having a cache that includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle. (*See* Abstract, Summary of the Invention, col. 2, ll.31-36)

As discussed above, Shen and Handy do not disclose an integrated coherent cache device as recited in claim 9 as amended, and by their dependency claims 16-17. Witt does not disclose an integrated cache coherent device. Therefore Applicants respectfully submit that claims 16-17 are allowable as depending from allowable base claim 9 given the arguments above.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 16-17 under 35 U.S.C. §103(a) is respectfully requested.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600**.

Respectfully submitted,

KENYON & KENYON

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